AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (Cancelled)

4. (Currently Amended) A microcomputer comprising:

a central processing unit;

a universal serial bus interface circuit which can be utilized as a debugging interface; and

an external bus interface circuit which can be connected to an external memory,

wherein the universal serial bus interface circuit includes a plurality of input buffers, and data is output from one of said input buffers in parallel with an input operation to another of said input buffers,

wherein the universal serial bus interface circuit receives a system program in a debugging mode, and the system program thus received can be output from the external bus interface circuit together with a memory access control signal,

wherein the microcomputer further comprises a direct memory access controller configured to perform a control to

transfer the received system program to a memory connected to the external bus interface, and

~~The microcomputer according to claim 3,~~ wherein a transfer source of the system program through the direct memory access controller is ~~an input buffer~~one of said input buffers of the ~~high speed serial communication interface~~ universal serial bus interface circuit.

5. (Currently Amended) A microcomputer comprising:

a central processing unit;

a universal serial bus interface circuit which can be utilized as a debugging interface; and

an external bus interface circuit which can be connected to an external memory,

wherein the universal serial bus interface circuit includes a plurality of input buffers, and data is output from one of said input buffers in parallel with an input operation to another of said input buffers,

wherein the universal serial bus interface circuit receives a system program in a debugging mode, and the system program thus received can be output from the external bus interface circuit together with a memory access control signal,

wherein the microcomputer further comprises:

a direct memory access controller configured to perform a control to transfer the received system program to the external memory connected to the external bus interface; and

~~The microcomputer according to claim 3, further comprising~~

a random access memory ~~capable of~~configured to temporarily ~~storing a~~store the system program received by ~~an input buffer~~ said one input buffer of the ~~high-speed serial communication interface circuit,~~ universal serial bus interface circuit,

wherein a transfer source of the system program through the direct memory access controller ~~being~~ is the random access memory.

Claim 6 (Cancelled)

7. (Currently Amended) A microcomputer comprising:

a central processing unit;

a high-speed serial communication interface circuit which can be utilized as a debugging interface; and

an external bus interface circuit which can be connected to an external memory,

wherein the high-speed serial communication interface circuit includes a plurality of input buffers therein, and

data is output from one of said input buffers in parallel with an input operation to another of said input buffers, and

the high-speed serial communication interface circuit is configured to receive a system program in the debugging mode, and the system program thus received can be output from the external bus interface circuit together with a memory access control signal,

wherein the microcomputer further comprises a debugging dedicated low-speed serial communication interface circuit which is usable to input control data to control the high-speed serial communication interface circuit in the debugging mode, and

~~The microcomputer according to claim 6, wherein~~ the debugging dedicated low-speed serial communication interface circuit is usable in place of the high-speed serial communication interface circuit for receiving the system program ~~in place of the high-speed serial communication interface circuit~~ in the debugging mode.

8. (Currently Amended) The microcomputer according to claim [[6]] 7, wherein the debugging dedicated low-speed serial communication interface circuit is based on JTAG protocol and ~~has~~ includes a data register.

9. (Currently Amended) The microcomputer according to claim [[1]] 7, further comprising a trace control circuit, the trace control circuit successively storing, as trace information, an internal state obtained when the central processing unit executes the system program.

10. (Original) The microcomputer according to claim 9, wherein the high-speed serial communication interface circuit can be utilized for an external output of the trace information.

Claim 11 (Cancelled)

12. (Currently Amended) A method of developing a system program which is to be executed by a target device using a host computer, an emulator, and the target device, comprising:

a first process of storing a first system program portion output through high-speed serial communication by the host computer in a buffer of a two-plane buffer as a processing to be carried out by the emulator;

a second process of transmitting a second system program portion stored in another buffer of the two-plane

buffer to the target device through low-speed serial communication in parallel with the first process; and

a third process of carrying out a handshake control of the low-speed serial communication with the target device, ~~The method for developing a system program according to claim 11,~~

wherein the second system program portion output from ~~the~~ said another buffer is transmitted through the low-speed serial communication to the target device via ~~an~~ a FIFO buffer having a storage capacity which is equal to or larger than that of ~~one of the buffers~~said another buffer in the second ~~processing~~process, and

a transmission from the FIFO buffer to the target device is carried out in response to a transmission permission sent from the target device, thereby suppressing a transfer from ~~the~~ said another buffer to the FIFO buffer in response to a full state of the FIFO buffer in the third ~~processing~~process.

13. (Currently Amended) A microcomputer having a user mode and a debugging mode, comprising:

a central processing unit;

a universal serial bus interface circuit;

~~an~~ a ROM retaining a first debugging control program;

~~an~~ a RAM; and

an external bus interface circuit,

wherein the universal serial bus interface circuit has a predetermined endpoint buffer circuit which can be utilized in the debugging mode, the predetermined endpoint buffer circuit has a pair of buffers which can be operated in parallel, and one of the buffers can be caused to carry out an input operation and the other buffer can be caused to carry out an output operation in parallel therewith, and

when the debugging mode is designated in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface circuit, the second debugging control program thus received is stored in the RAM, and a transition to an execution of the second debugging control program stored in the RAM is made.

14. (Currently Amended) The microcomputer according to claim 13, further comprising a buffer RAM and a direct memory access controller,

wherein the central processing unit ~~causing~~ causes the direct memory access controller to transfer the second

debugging control program received by the universal serial bus interface circuit to the buffer RAM in response to a download request command received by the universal serial bus interface circuit in accordance with the second debugging control program.

15. (Currently Amended) The microcomputer according to claim 14, wherein the central processing unit causes the direct memory access controller to carry out a control to transfer [[a]] the second debugging control program transmitted to the buffer RAM through ~~an~~ the external bus interface circuit to an outside in response to a transfer request command received by the universal serial bus interface circuit in accordance with the second debugging control program.

16. (Original) The microcomputer according to claim 13, wherein the central processing unit makes a transition to the user mode in response to a mode control command in an execution state of the second debugging control program, and

the central processing unit fetches an instruction through the external bus interface circuit in the user mode.

17. (Currently Amended) A microcomputer comprising:

a central processing unit;

a universal serial bus interface circuit;

~~an~~ a ROM retaining a first debugging control program;

a buffer RAM; and

an external interface circuit,

wherein the universal serial bus interface circuit has a predetermined endpoint buffer circuit, the predetermined endpoint buffer circuit has a pair of buffers which can be operated in parallel, and one of the buffers can be caused to carry out an input operation and the other buffer can be caused to carry out an output operation in parallel therewith, and

in a power-on reset, the central processing unit executes the first debugging control program to initialize the universal serial bus interface circuit to be operable, a second debugging control program is received by the universal serial bus interface circuit, the second debugging control program thus received is stored in the buffer RAM, and the second debugging control program stored in the buffer RAM is output through the external interface circuit.

18. (Original) The microcomputer according to claim 17, further comprising a direct memory access controller, the

direct memory access controller transferring the second debugging control program from the buffer RAM to an outside through the external interface circuit in accordance with a transfer control condition set by the central processing unit.